R & D Electronics (Pty) Ltd

QBC-QBX

UNIVERSAL MULTIBUS* CARD
FOR QBX FUNCTIONS

Product:÷ QBC÷QBX
Product Number:÷ 3Ø1
Manual Number:÷ 3Ø1÷Ø1

Chapter	Rev	Note
All	1.Ø	1
3,4,5	1.1	2

Notes:÷
1.Original Document
2.Changes due to rework of board, supply of parts

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CHAPTER 1
GENERAL

Introduction

The QBC-QBX is one of a growing range of boards supporting the SBX bus manufactured by R & D Electronics. This board is designed to provide a host board for up to four SBX bus compatible boards. Aside from the support logic the QBC-QBX has no function. Its concept is somewhat akin to the EPROM in that it has no function, its personality is totally user configurable to that required by the designer. In addition it allows a versatile adaption as the QBX boards may be memory mapped instead of I/O mapped.

Description

The QBC-QBX is an original product that allows expansion of Multibus based systems with a greater degree of flexibilty that has hitherto been difficult to achieve. Several manufacturers produce Multibus boards with SBX bus compatible connectors, but these are all either CPU boards (not allowing access to other CPUs in a multiprocessor environment) or complex functions (expensive and possibly unneeded). Currently three is the maximum number of SBX sockets on a CPU board. To add further functions requires the addition of another Multibus board. The QBC-QBX fulfils this need by allowing a multitude of functions to be implemented by merely using SBX modules. It even allows the use of a CPU board that does not support the SBX bus, allowing retrofits to existing designs and usage of stock boards that would not be otherwise used.

The QBC-QBX may be configured as memory mapped I/O (up to 20 bits of address space) or I/O mapped I/O. It only supports 8 bit SBX modules but most 16 bit CPU boards will support 8 bit data transfers. The QBC-QBX also does not support the iLBX bus and the P2 connector is configured for additional functions that may be similar to those detailed in Intel literature (mentioned later).

Up to 4 single sized SBX compatible modules may be mounted on the QBC-QBX; or 3 single and 1 double; or 2 single and two double sized modules.

Equipment Supplied

The QBC-QBX is shipped in a padded package. No other parts are supplied.

Specifications

Access Time:
Programmable XACK/ time Ø-9ØØns (nominally 4ØØ-5ØØns) see chap.2

Addressing Range:
The QBC-QBX may be configured as memory mapped I/O or I/O mapped I/O. Up to 2Ø bits of address information may be presented. Any socket that is not used is automatically mapped out of the range allowing the address space to be used elsewhere in the system.

Interface:
System Bus Compatible with the Multibus specifications. IEEE P796 bus compliance D8 M2Ø I16 VO L.

Four of: 8 bit QBX bus sockets

P2 edge connector, 6Ø way, Ø.1 inch spacing, compatible with Intel application note AP28A, or users own requirements.

P3 edge connector, 26 way, Ø.1 inch spacing, - can be wired for DMA capabilty.

Environment:
Operating Temperature Ø-55 degrees Celsius, humidity to 9Ø% non-condensing.

Power Requirements:
(Exclusive of QBX power requirements)
5 Volts +/- 5% @ 1.386 Amps
12 volts +/- 5% @ 12 mAmps

Size:

Width	3Ø4.8 mm (12 in)
Length	171.5 mm (6.75 in)
Thickness	1.27 mm (Ø.5 in)

CHAPTER 2
PRINCIPLE OF OPERATION

Introduction

This chapter describes the hardware operation of the QBC÷QBX. It is assumed that the user is familiar with the Intel Publications "Intel MULTIBUS Interfacing" (AP28A), the iSBX bus specification (publication 142686÷ØØ1) and the "IEEE Proposed Microcomputer System Bus Standard ÷ P796 Bus". This chapter should be read in conjunction with the circuit diagram in Chapter 5.

MULTIBUS Interface

The QBC÷QBX may be configured as a memory mapped I/O or I/O mapped I/O slave module. It may be used with up to 2Ø addressing bits. The user is referred to the above documents for the relevant timing diagrams and data associated with the SBX and Multibus.

The last 4 addresses of a 16 Mbyte address space, A14÷A17 (in hexadecimal notation) are not supported. These signals are present on the P2 connector and are brought to link pins so that if these addresses are present in the system, provided that the QBC÷QBX is configured for I/O mapped I/O, no problem will arise.

Address Decoding

The QBC÷QBX will support up to 4 QBX (QBX is R & D Electronics' implementation of the Intel SBX bus) modules. Since each module reserves 16 address locations this means that a maximum of 64 locations must be accessible on card. As a result board select ignores address lines AØ to A5 inclusive, leaving up to 14 address lines to be decoded. The Multibus must support 16 or 2Ø bit memory addressing, or 8 or 16 bit I/O addressing. With the hardware supplied addresses may be rendered irrelevant 4 bits at a time.

The 64 locations must be contiguous, but if a QBX module is not installed then those 16 bits (even if they are in the middle of these 64 locations) may be allocated for use elsewhere in the system.

The address bits (A8/÷A13/) are fed to 16 pin sockets, 4 bits at a time. If the 4 DIP jumpers are installed in the upper four positions of the socket (shorting pins 1÷16, 2÷15, 3÷14, 4÷13) these bits are fed through to the "A" inputs of a comparator. If the four jumpers are installed in the lower position (shorting 5÷12, 6÷11, 7÷1Ø, 8÷9) then the corresponding "A" and "B" input bits of the comparator are shorted together and so these inputs are effectively disabled. These sockets are U18, U21, and U22. Individual bits may be set to don't care conditions by treating the four jumpersseparately. See Table 2.1.

Address Line	Socket	Pin
A13/	U18	1
A12/	U18	2
A11/	U18	3
A1Ø/	U18	4
AF/	U21	1
AE/	U21	2
AD/	U21	3
AC/	U21	4
AB/	U22	1
AA/	U22	2
A9/	U22	3
A8/	U22	4

Table 2.1
Address Jumper Inputs

The "B" inputs to the comparators (U19 and U23) have pull up resistors connected to switches, that when closed pull these lines to ground. The address complements are available on the Multibus and these are fed directly into the comparator "A" inputs. The corresponding programming switch should be closed shorting that "B" input to ground for a high on the address bit. e.g. If A7 is required to be a logical "1" then the corresponding switch should be closed setting the "B" input to a logical "Ø" as the signal presented to the comparator will be inverted.

When the input address matches the programmed address the outputs of U19 and U23 go low. These two signals are fed into an OR gate (2 OR gates in fact for drive considerations). The output of this gate is the board select that enables the rest of the logic.

Individual Module Selects

Individual Chip selects (CSØ and CS1) for each QBX module are derived from addresses A3, A4, and A5. These address lines are buffered and fed into a 3 to 8 line decoder. Odd and even output pairs (YØ and Y1) from this decoder when gated with the board select signal, through additional gating (for speed requirements), provides CSØ/ and CS1/ respectively.

Buffer Enables

In order to comply with the current drive requirements of the SBX bus two data bus buffers are required. The devices used (8287) still leave the data bus interface within the Multibus drive specifications. Each buffer caters for two QBX modules. Address lines A5 and A4 are used to provide a module select signal via a 3 to 8 decoder. Each of these outputs are gated with the MPST/ of the respective QBX modules. Where the module is present one or the other of the data bus buffers is enabled. The natural direction of data is onto the board. When the RD (memory or I/O) is active the direction of data flow is reversed.
XACK/

The handshake function XACK/ is used to extend access time to the QBX boards on a general basis (via a programmable jumper) or on an individual basis using the MWAIT/ signal from the QBX module.

When any one of the modules is selected and a write or read command initiated (CMD/) a serial to parallel shift register (U16) is enabled along with the three state buffer (U14) driving the XACK line of the Multibus. All the outputs of this shift register are originally at zero. At each positive clock edge a logical one is shifted along the outputs. One of these outputs is jumpered to pin 12 of an eight input NAND gate (U13). A high on this input enables the NAND gate and by jumpering only one output from the shift register to this input allows a programmable time delay in accessing all the modules. The clock signal is normally derived from the BCLK (10 MHz) Multibus signal. Table 2.2 lists the time delays associated with each output. The minimum write time of a normal QBX module is 300nS. So combined with the Multibus delays and setups the minimum setting should be the jumper shorting pins 5 - 12 (a minimum of 400nS) of the socket U15. Wait states from the QBX modules are gated with this output to extend the XACK/ signal.

Output	Short pins on U15	Time (10 MHz clock)
A	1 - 16	0 - 100 nS
B	2 - 15	100 - 200 nS
C	3 - 14	200 - 300 nS
D	4 - 13	300 - 400 nS
E	5 - 12	400 - 500 nS
F	6 - 11	500 - 600 nS
G	7 - 10	600 - 700 nS
H	8 - 9	700 - 800 nS

Table 2.2
Timing of XACK/

If the BCLK signal is not available or at the wrong frequency the user may optionally add an Intel 8224 clock generator (U29), plus crystal capacitor (C17) and a 74LS74A (U28) to provide another clock. LK3 through LK6 may be used to set up this frequency.

Interrupt

The interrupts from the modules are brought out to links. These may be jumpered to inverters and these in turn may be jumpered to the 8 interrupt lines of the Multibus. These inputs may also be combined to economise on interrupt lines utilising U27. Unused inputs to U27 may be pulled up using R13. The interrupt inverters are open collector 7416s, and if this is done it would be prudent to replace these with 7404s. In addition the user software would have to poll to find the source of the interrupt, and reset it.

OPT0 and OPT1

The outputs OPTØ and OPT1 from each module are brought out to jumpers.

D.M.A.

All the outputs related to Direct Memory Access from each module are brought out to a third edge connector P3 via some jumpers.

P2 Connector

Since the QBC÷QBX is essentially an I/O support module there is no call for support of the iLBX bus. This bus uses the P2 connector as well. If the LBX bus is present in the system then it must not be connected to the P2 connector of the QBC÷QBX. The P2 connector of the QBC÷QBX is configured to support the optional format as presented in the Intel application note AP28A.

CHAPTER 3
PROGRAMMING INFORMATION

Introduction

This chapter provides all the information to "programme" the QBC-QBX. There is no software setup at all, only programming of switches, links and jumpers.

I/O or Memory Mapping

The board must first be configured as I/O mapped I/O or memory mapped I/O. This information is given in Table 3.1.

Mapping Function	Short Pins on Socket 1
I/O Write	1 - 8
I/O Read	2 - 7
Memory Write	3 - 6
Memory Read	4 - 5

Table 3.1
I/O Space Mapping

For convenience a two way jumper is provided. When the jumper is installed in the upper half of the 8 pin socket U1, the unit is configured for I/O mapped I/O. With this jumper installed in the lower half of U1 the QBC-QBX is configured for memory mapped I/O.

Address Setup (I/O mapping)

(i) 8 bit I/O mapping
Set the jumpers up so that the conditions in Table 3.2 are met.

Note that using the 4 way jumpers installing in the upper half of the socket enables the respective 4 address bits,whilst in the lower half disables those address bits.

Socket	Open Pins	Short Pins
U18	1-16	5-12
U18	2-15	6-11
U18	3-14	7-10
U18	4-13	8- 9
U21	1-16	5-12
U21	2-15	6-11
U21	3-14	7-10
U21	4-13	8- 9
U22	1-16	5-12
U22	2-15	6-11
U22	3-14	7-10
U22	4-13	8- 9

Table 3.2
Jumper Configuration 8 bit I/O Mapped

The address switch should be set up as in Table 3.3.

Function	Switch Pack	Switch #	State
A13/	U2Ø	1	X
A12/	U2Ø	2	X
A11/	U2Ø	3	X
A1Ø/	U2Ø	4	X
AF/	U2Ø	5	X
AE/	U2Ø	6	X
AD/	U2Ø	7	X
AC/	U2Ø	8	X
AB/	U24	1	X
AA/	U24	2	X
A9/	U24	3	X
A8/	U24	4	X
A7/	U24	5	On=1, Off=Ø
A6/	U24	6	On=1, Off=Ø

Table 3.3
Switch Settings for 8 Bit I/O Mapping (X- don't care)

(ii) 16 bit I/O mapping
Set the jumpers up so that the conditions in Table 3.4 are met:

Socket	Open Pins	Short Pins
U18	1-16	5-12
U18	2-15	6-11
U18	3-14	7-1Ø
U18	4-13	8- 9
U21	1-16	5-12
U21	2-15	6-11
U21	3-14	7-1Ø
U21	4-13	8- 9
U22	5-12	1-16
U22	6-11	2-15
U22	7-1Ø	3-14
U22	8- 9	4-13

Table 3.4
Jumper Configuration 16 bit I/O mapped
(12 bit address space)

Note that using the 4 way jumpers installing in the upper half of the socket enables the respective 4 address bits,whilst in the lower half disables those address bits.

The address switches should be set up as in Table 3.5.

Note: U2Ø is split into 2 8 pin units. The numbering in this documentation is consistent with a a single 16 pin unit. i.e. pin 1 of U2ØB is listed as pin 5 of the imaginary U2Ø. Switch 1 of U2ØB is switch 5 of the imaginary U2Ø and so forth.

Function	Switch Pack	Switch #	State
A13/	U20	1	X
A12/	U20	2	X
A11/	U20	3	X
A10/	U20	4	X
AF/	U20	5	X
AE/	U20	6	X
AD/	U20	7	X
AC/	U20	8	X
AB/	U24	1	On=1, Off=0
AA/	U24	2	On=1, Off=0
A9/	U24	3	On=1, Off=0
A8/	U24	4	On=1, Off=0
A7/	U24	5	On=1, Off=0
A6/	U24	6	On=1, Off=0

Table 3.5
Switch Settings for 16 Bit I/O Mapping
(X- don't cares)

Address Setup (memory mapping)

(i) 16 bit memory mapping
Set the jumpers up so that the conditions in Table 3.6 are met:

Socket	Open Pins	Short Pins
U18	1-16	5-12
U18	2-15	6-11
U18	3-14	7-10
U18	4-13	8- 9
U21	5-12	1-16
U21	6-11	2-15
U21	7-10	3-14
U21	8- 9	4-13
U22	5-12	1-16
U22	6-11	2-15
U22	7-10	3-14
U22	8- 9	4-13

Table 3.6
Jumper Configuration 16 bit Memory Mapped

Note that using the 4 way jumpers installing in the upper half of the socket enables the respective 4 address bits,whilst in the lower half disables those address bits.

The address switch should be set up as in Table 3.7.

Function	Switch Pack	Switch #	State
A13/	U20	1	X
A12/	U20	2	X
A11/	U20	3	X
A10/	U20	4	X
AF/	U20	5	On=1, Off=0
AE/	U20	6	On=1, Off=0
AD/	U20	7	On=1, Off=0
AC/	U20	8	On=1, Off=0
AB/	U24	1	On=1, Off=0
AA/	U24	2	On=1, Off=0
A9/	U24	3	On=1, Off=0
A8/	U24	4	On=1, Off=0
A7/	U24	5	On=1, Off=0
A6/	U24	6	On=1, Off=0

Table 3.7
Switch Settings for 16 Bit Memory Mapping
(X- don't cares)

(ii) 20 bit memory mapping
Set the jumpers up so that the conditions in Table 3.8 are met:

Socket	Open Pins	Short Pins
U18	5-12	1-16
U18	6-11	2-15
U18	7-10	3-14
U18	8- 9	4-13
U21	5-12	1-16
U21	6-11	2-15
U21	7-10	3-14
U21	8- 9	4-13
U22	5-12	1-16
U22	6-11	2-15
U22	7-10	3-14
U22	8- 9	4-13

Table 3.8
Jumper Configuration 20 bit Memory Mapped

Note that using the 4 way jumpers installing in the upper half of the socket enables the respective 4 address bits,whilst in the lower half disables those address bits.

The address switches should be set up as in Table 3.9.

Function	Switch Pack	Switch #	State
A13/	U2Ø	1	On=1, Off=Ø
A12/	U2Ø	2	On=1, Off=Ø
A11/	U2Ø	3	On=1, Off=Ø
A1Ø/	U2Ø	4	On=1, Off=Ø
AF/	U2Ø	5	On=1, Off=Ø
AE/	U2Ø	6	On=1, Off=Ø
AD/	U2Ø	7	On=1, Off=Ø
AC/	U2Ø	8	On=1, Off=Ø
AB/	U24	1	On=1, Off=Ø
AA/	U24	2	On=1, Off=Ø
A9/	U24	3	On=1, Off=Ø
A8/	U24	4	On=1, Off=Ø
A7/	U24	5	On=1, Off=Ø
A6/	U24	6	On=1, Off=Ø

Table 3.9
Switch Settings for 2Ø Bit Memory Mapping (X- don't cares)

Module Addressing

Within the 64 memory locations each module occupies 16 locations. Table 3.1Ø tabulates this space allocation. The most significant 12 bits are not shown as they are dependant on mapping and are dealt with above. The letters PQ denote the address setting for A7/ and A6/. X denotes a don't care condition meaninig an address within the range. **Note:** The addresses presented here are the true addresses and not the complements.

Module	A7	A6	A5	A4	A3	A2	A1	AØ
A- CSØ	P	Q	Ø	Ø	Ø	X	X	X
A- CS1	P	Q	Ø	Ø	1	X	X	X
B- CSØ	P	Q	Ø	1	Ø	X	X	X
B- CS1	P	Q	Ø	1	1	X	X	X
C- CSØ	P	Q	1	Ø	Ø	X	X	X
C- CS1	P	Q	1	Ø	1	X	X	X
D- CSØ	P	Q	1	1	Ø	X	X	X
D- CS1	P	Q	1	1	1	X	X	X

Table 3.1Ø
QBX module addresses

XACK/ setting

The setting of the jumper in socket U15 should be from 5 -12, an XACK/ time of 4ØØ-5ØØnSec. Unless all the QBX modules have a faster access time than the nominal SBX bus specifications, or those that don't have wait state generators this time should not

be shortened. It can be extended if required, but the SBX module should have its own Wait state generator if this is the case. Table 2.2 provides the timing relationships.

Interrupt

The two interrupt lines from each module are brought out to two jumper locations. Associated with each location is a another jumper, connected to the input of an inverter. The output of this inverter may be connected to one of the Multibus lines INTØ/ to INT7/. The output may also be connected to the input of an 8 input AND gate so that several interrupt lines may be combined. The output of this AND configuration may be connected to one of the Multibus interrupt lines. Table 3.11 lists all the relevant jumpers. Whilst the jumpers are organised physically on the board in a logical pattern, there is no reason why they may not be connected as the user requires.

QBX function	Invrtr In	Invrtr Out	INT	AND input
INT1 A - 52	60	68	INT7/ -77	36
INTØ A - 53	61	69	INT6/ -78	37
INT1 B - 54	62	70	INT5/ -79	38
INTØ B - 55	63	71	INT4/ -80	39
INT1 C - 56	64	72	INT3/ -81	40
INTØ C - 57	65	73	INT2/ -82	41
INT1 D - 58	66	74	INT1/ -83	42
INTØ D - 59	67	75	INTØ/ -83	43

Table 3.11
Jumper Locations for Interrupt Functions
Jumper 76 - output of AND configuration

OPTØ and OPT1

The SBX standard allows user configured outputs called OPTØ and OPT1. These two outputs are brought out from each module to a jumper location. They may be wired to the interrupt lines, the lines on the P2 connector or even the lines on the P3 connector. Table 3.12 lists the outputs and their associated jumper numbers.

Function	Jumper Label
OPT1- A	44
OPTØ- A	45
OPT1- B	46
OPTØ- B	47
OPT1- C	48
OPTØ- C	49
OPT1- D	50
OPTØ- D	51

Table 3.12
OPTØ/1 Jumpers

D.M.A.

The QBC-QBX does not support DMA directly but does allow the user to bring these signals off the board via the connector P3. To do this several jumper locations must be connected. Table 3.13 provides a summary of the DMA associated signals while Table 3.14 describes the allocation of the edge connector P3 to jumper locations.

Function	Jumper location
MDRQT- A	13
MDACK/- A	15
TDMA- A	17
MDRQT- B	19
MDACK/- B	21
TDMA- B	23
MDRQT- C	25
MDACK/- C	27
TDMA- C	29
MDRQT- D	31
MDACK/- D	33
TDMA- D	35

Table 3.13
DMA jumper functions

P3 connector pin	Jumper label
1	(GND)
2	(GND)
3	12
4	(GND)
5	18
6	11
7	24
8	10
9	30
10	9
11	32
12	8
13	26
14	7
15	20
16	6
17	14
18	5
19	18
20	4
21	28
22	3
23	22
24	2
25	16
26	1

Table 3.14
P3 to Jumper Label

P2 Connector

The connector P2 is configured to handle the suggested specifications listed in the Intel application note AP28A. Where there are the same functions on two or more of the connector pins (e.g. pins 23 and 24 +15V) these are shorted together. Except for the case of ground all pins are brought to jumper locations. The ground is tied to the system ground. Table 3.15 relates the pins of P2 to the jumper labels. The function names are the optional signals taken from the Intel application note.

Connector P3 Pin	Jumper Label	Function
1		\ Gnd
2		/
3	\86	\ 5VB +5V battery
4	/	/
5	121	
6	87	VCCPP +5V pulsed power
7	\88	\ -5VB -5V battery
8	/	/
9	123	
10	122	
11	\89	\ 12VB +12V battery
12	/	/
13	90	PFSR/ Power fail sense reset
14	124	
15	\91	\ -12VB -12V battery
16	/	/
17	92	PFSN/ Power fail sense
18	93	ACLO AC low
19	94	PFIN/ Power fail interrupt
20	95	MPRO/ Memory protect
21		\ Gnd
22		/
23	\96	\+15V
24	/	/
25	\97	\-15V
26	/	/
27	98	PAR1/ parity 1
28	99	HALT/ bus master halt
29	100	PAR2/ parity 2
30	101	WAIT/ Bus master wait state
31	125	
32	102	ALE Bus master ALE
33	110	
34	111	
35	126	
36	112	
37	127	
38	103	AUX RESET/ Reset switch
39	128	
40	113	
41	114	
42	104	

	43	129			
	44	105			
	45	115			
	46	106			
	47	116			
	48	130			
	49	107			
	50	131			
	51	132			
	52	117			
	53	118			
	54	108			
	55	109			
	56	133			
	57	134			
	58	119			
	59	135			
	60	120			

Table 3.15
P2 to Jumper Label

CHAPTER 4
PREPARATION FOR USE

Introduction

This chapter provides information on the installation of a QBX board on a host QBC-QBX board.

Unpacking

The QBC-QBX is shipped in a padded packet.On receipt of the package inspect immediately for signs of damage, water or any other signs of mishandling. If there are any of these signs contact your carrier or his agent, or the local R & D Electronics representative. If you do open the package, please retain the packaging.

Configuration

Setup the address and mapping jumpers and switches as dealt with in chapters 2 and 3. Configure the jumper connections as required. This may be attained by fitting wire wrap posts to the pads and then wire-wrapping these or by soldering directly to the board.

Mounting

The QBC-QBX can hold up to 4 single sized SBX modules or one double sized and 3 single sized or 2 single sized and 2 double sized SBX boards. You will notice on the board that their are in fact 5 sockets but that two of them are denoted as "B" and "B' ". These two sockets are connected in parallel i.e. there is no difference electrically between them. The reason is to cater for double sized SBX boards. If a double sized SBX module is mounted on socket A, the "B" sockets is obscured. The "B' "socket is now available for either a single or double SBX board. Table 4.1 describes the allocation of sockets for a full complement of SBX boards.

Socket	Single	Double
A	x	x
B	x	
B'	x	x
C	x	
D	x	

Table 4.1
Optimal allocation of SBX module sizes

There is one limitation on the back board if double sized and mounted on socket B'. One of the required mounting holes does not line up. Since the other three holes do no real problem is envisaged.

Any 8 bit SBX compatible board will fit on the QBC-QBX. Simply mount the board in the desired socket and affix as many spacers as required as per the instructions of the specific SBX module. Mount the spacer in the hole corresponding to the mounting hole/s on the QBC board. The SBX board should now be mounted on the mating connector and affixed to the QBC-QBX with the remaining screw.

When a QBX module is mounted on the QBC-QBX card, the resulting structure occupies an additional card slot above the QBC card. Bear this in mind when you allocate slots in a cardframe.

Installation

Install the configured QBC-QBX in the card cage with the **power off**. Mate the board with the back plane connectors. If the chassis has fixings to secure the card then apply these fixings.

Edge Connector

If it is used mate the edge connector to P3 on the QBC-QBX board.

CHAPTER 5
SERVICE

Introduction

This chapter provides a parts list and a schematic diagram of the QBC÷QBX.

Parts List

Semiconductors:

U2,17,26	FAST hex inverter	74FØ4
U4	Schottky 2 input NOR	74SØ2
U3,5	Schottky 2 input NAND	74SØØ
U6	Schottky 4 input NAND	74S2Ø
U7,9,11,12	Schottky 2 input OR	74S32
U8,1Ø	Schottky 3 to 8 decoder	74S138
U13,27	L.P. Schottky 8 inupt NAND	74LS3Ø
U14	L.P. Schottky 3 state buffer	74LS125
U16	L.P. Schottky sr to pll s.r.	74LS164
U19,23	FAST octal comparator	74F521
U28 *	L.P. Schottky D type FF	74LS74A
U29 *	Clock generator	8224
U3Ø,31	Bus buffers	8287/DP83Ø3
U32,33	O.C. inverter	7416

* Not provided

Capacitors:

C1,2,5,7,8,9, 12,14,15,19, 21,22,25,27,28, 31,33,36,37,38,39 41÷54	ceramic 5Ø Volt	Ø.1uF
C3,4,6,1Ø,11, 13,16,18,2Ø, 23,24,26,29,3Ø,32	tantalum 16 volt	1uF
C34,35	tantalum 16 volt	1ØuF

Resistors:

RN1,2	SIL resistor array Epitek 6.8K	L1Ø9÷682÷G
R1,2,3,4, 5,6,7,8,9, 1Ø,11,12,13	1/4W 5%	1 Kohm
R14	1/4W 5%	4.7 Kohm

Connector:

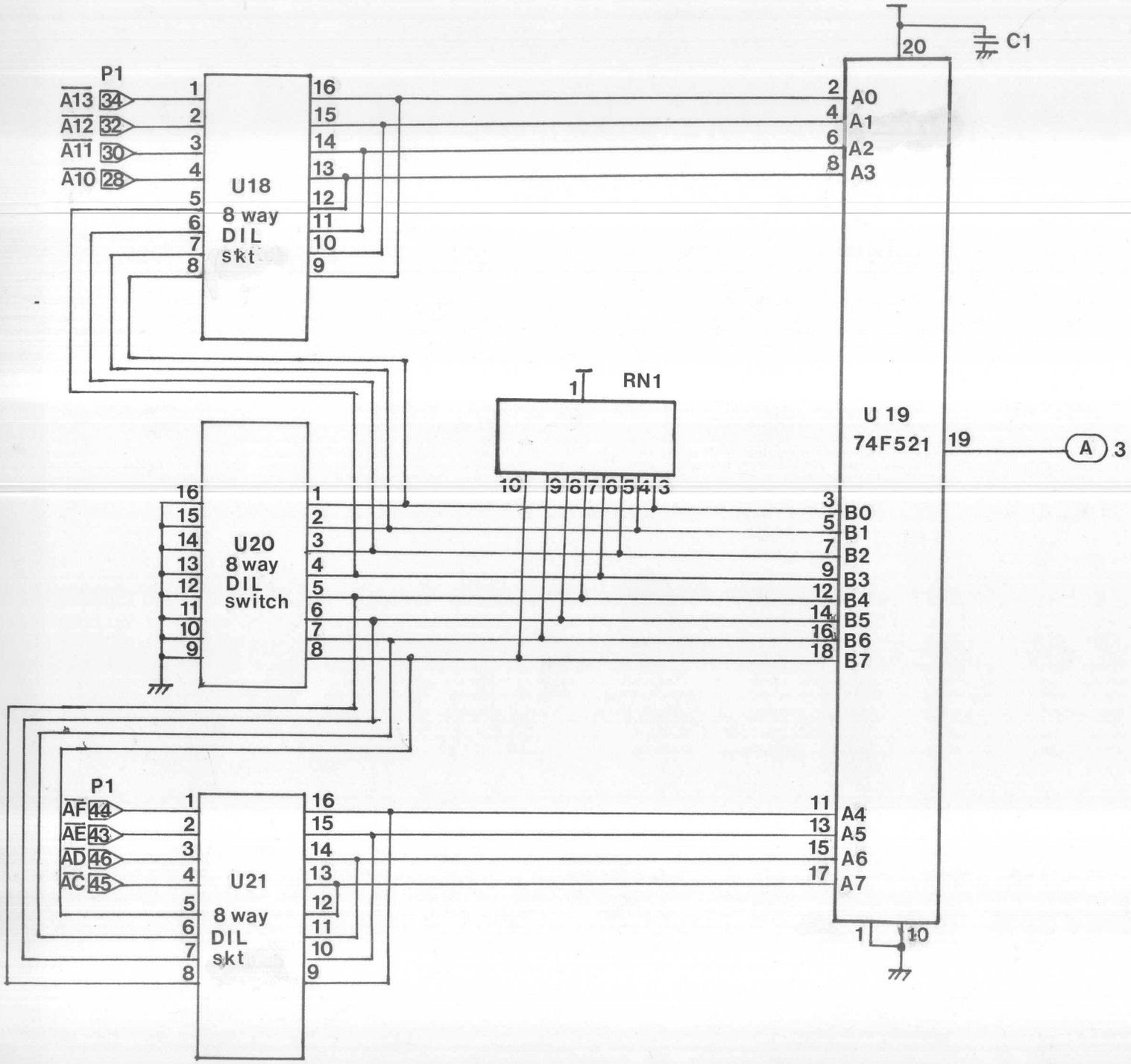
A,B,B' C,D	Viking 36 way SBX socket	LMRØ1KH18AØ1

Sundries:

U1	8 pin DIL socket
P1	2 single way shorting jumpers for U1
U18,21, 22,15	16 pin DIL socket
P18,21,22	4 single way shorting jumpers for U18,20,22
P15	single way shorting jumper for U15
U20a,b	4 way DIL switches
U24	8 way DIL switches
X1 *	User supplied crystal
	SCANBE card ejectors S203

Unused Parts:

C40
U25



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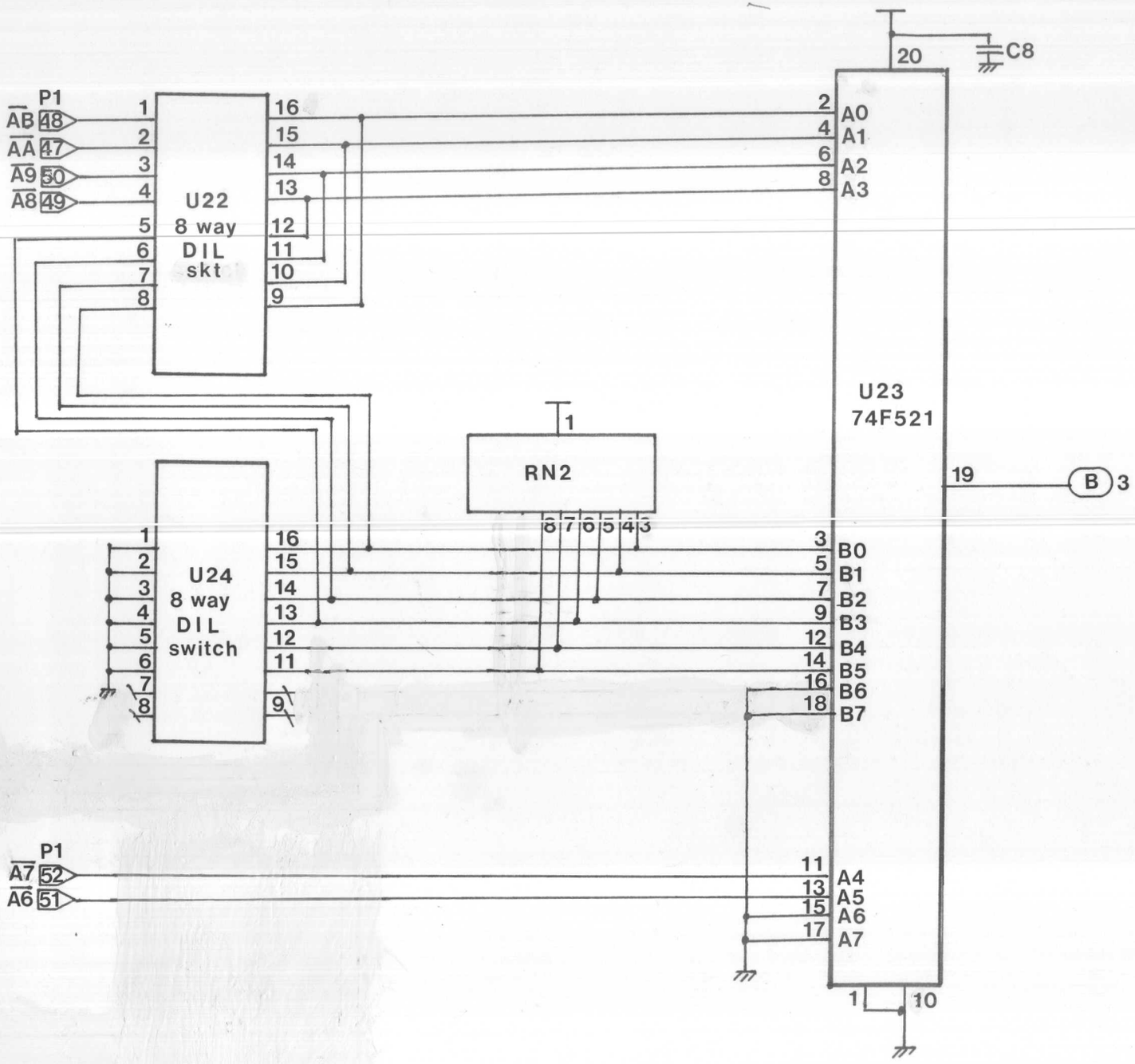
Upper Address Decode
Rev 1.1



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3001 – 02

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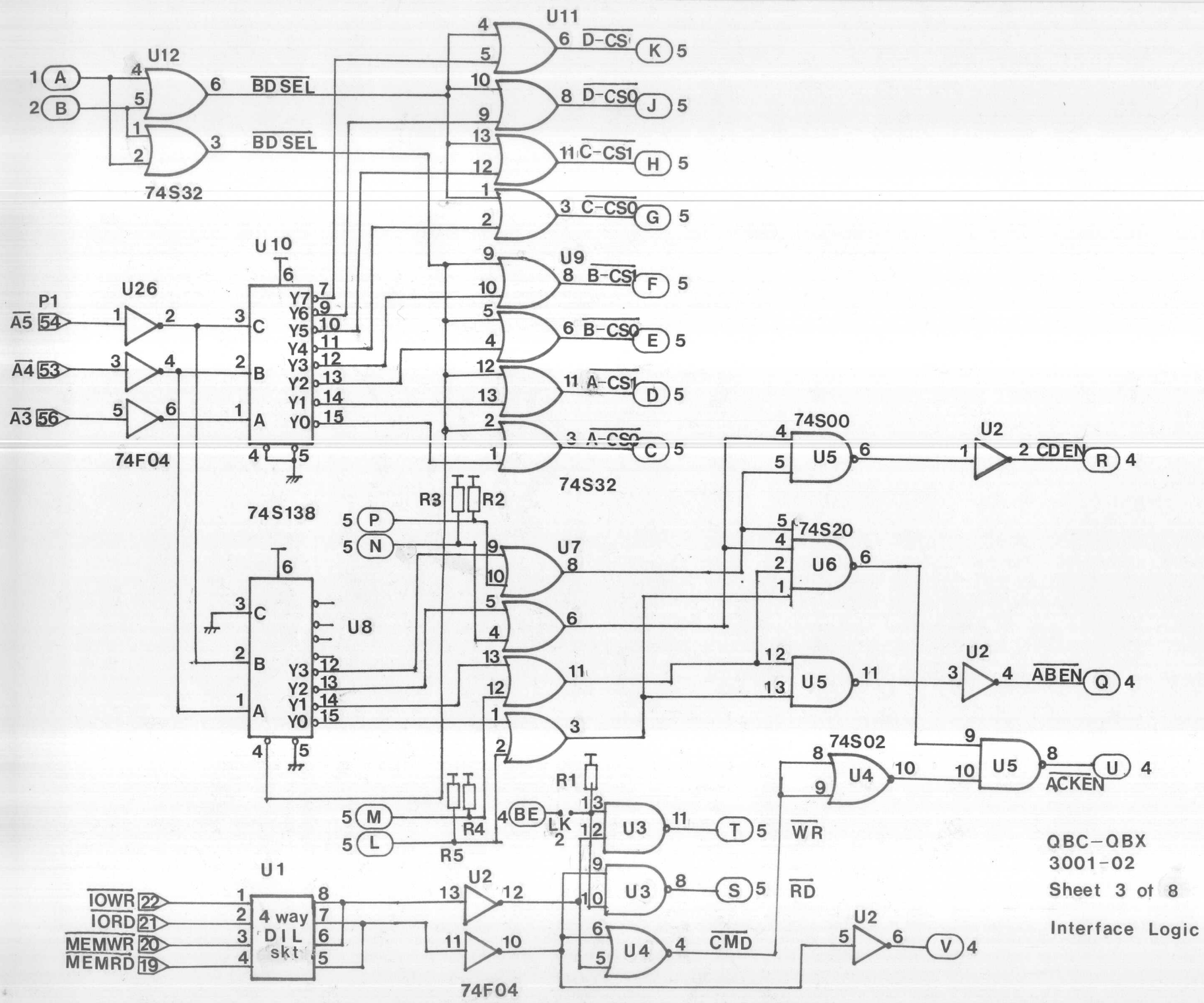
Lower Address Decode



QBC-QBX
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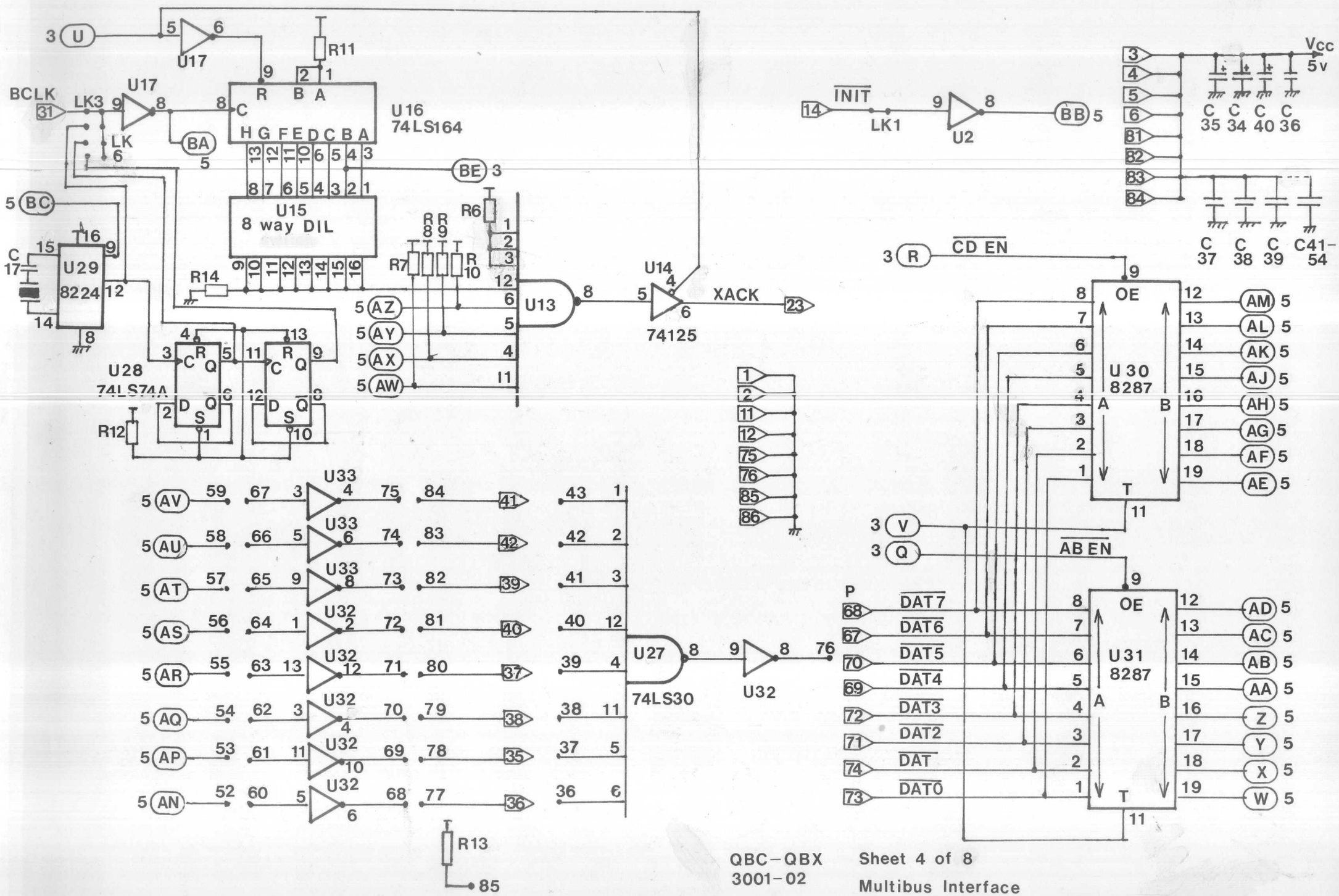
Interface Logic



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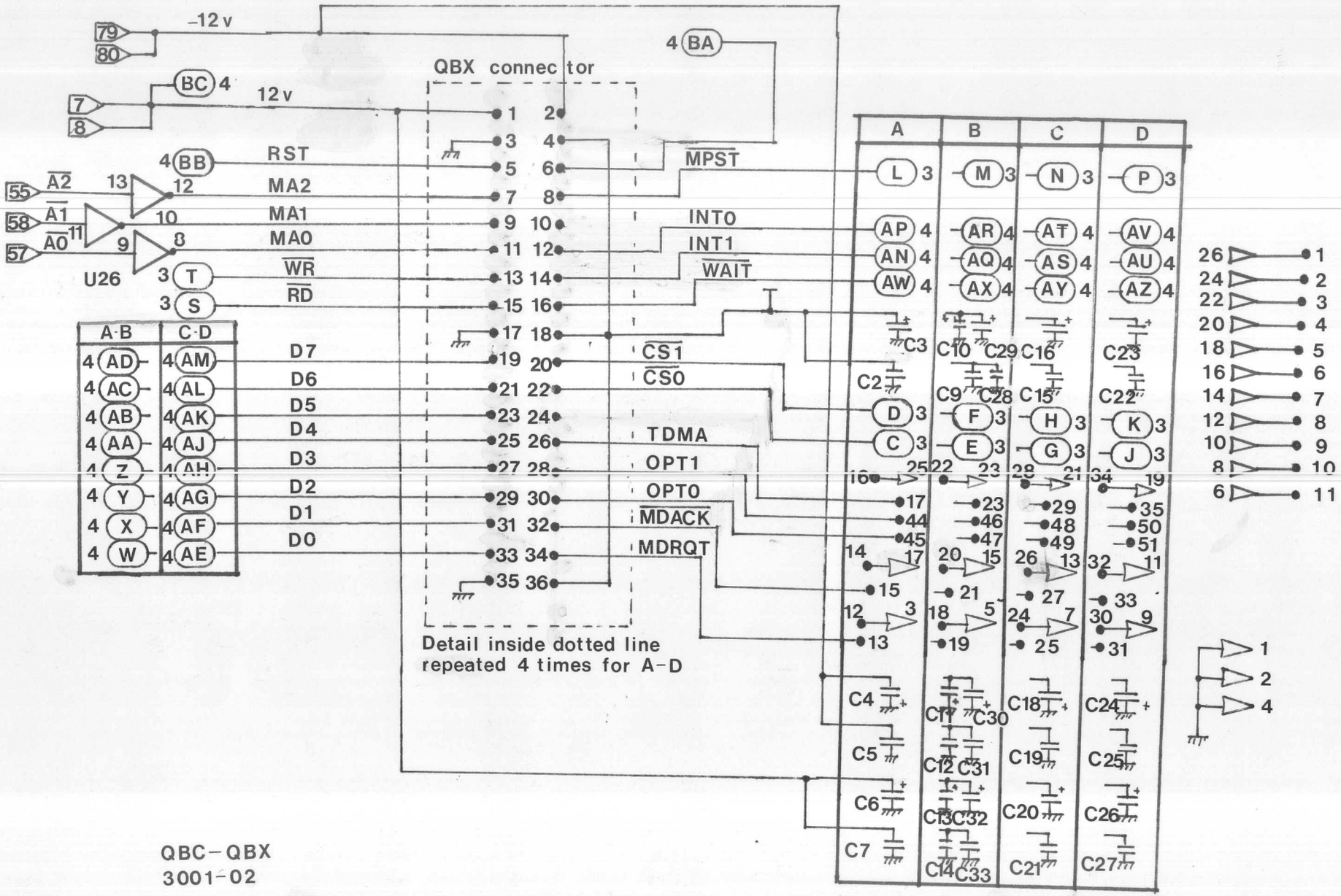
Multibus Interface



QBC-QBX
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QBX bus connectors

Jumper Label	Function
1	General purpose pin 26 P3
2	" 24
3	" 22
4	" 20
5	" 18
6	" 16
7	" 14
8	" 12
9	" 10
10	" 8
11	" 6
12	Associated with jumper 13 to pin 3 P3
13	MDRQT/ socket A
14	Associated with jumper 15 to pin 17 P3
15	MDACK/ socket A
16	Associated with jumper 17 to pin 25 P3
17	TDMA socket A
18	Associated with jumper 19 to pin 5 P3
19	MDRQT/ socket B
20	Associated with jumper 21 to pin 15 P3
21	MDACK/ socket B
22	Associated with jumper 23 to pin 23 P3
23	TDMA socket B
24	Associated with jumper 25 to pin 7 P3
25	MDRQT/ socket C
26	Associated with jumper 27 to pin 13 P3
27	MDACK/ socket C
28	Associated with jumper 29 to pin 21 P3
29	TDMA socket C
30	Associated with jumper 31 to pin 9 P3
31	MDRQT/ socket D
32	Associated with jumper 33 to pin 11 P3
33	MDACK/ socket D
34	Associated with jumper 35 to pin 19 P3
35	TDMA socket D
36	Input to U27 - Combined Interrupt
37	Input to U27 - Combined Interrupt
38	Input to U27 - Combined Interrupt
39	Input to U27 - Combined Interrupt
40	Input to U27 - Combined Interrupt
41	Input to U27 - Combined Interrupt
42	Input to U27 - Combined Interrupt
43	Input to U27 - Combined Interrupt
44	OPT1 socket A
45	OPT0 socket A
46	OPT1 socket B
47	OPT0 socket B
48	OPT1 socket C
49	OPT0 socket C
50	OPT1 socket D
51	OPT0 socket C
52	INT1 socket A
53	INT0 socket A

54	INT1 socket B
55	INTØ socket B
56	INT1 socket C
57	INTØ socket C
58	INT1 socket D
59	INTØ socket D
6Ø	Inverter in-associated with jumpers 52 & 68
61	Inverter in-associated with jumpers 53 & 69
62	Inverter in-associated with jumpers 54 & 7Ø
63	Inverter in-associated with jumpers 55 & 71
64	Inverter in-associated with jumpers 56 & 72
65	Inverter in-associated with jumpers 57 & 73
66	Inverter in-associated with jumpers 58 & 74
67	Inverter in-associated with jumpers 59 & 75
68	Output inverter
69	Output inverter
7Ø	Output inverter
71	Output inverter
72	Output inverter
73	Output inverter
74	Output inverter
75	Output inverter
76	Multibus signal INT7/
77	Multibus signal INT6/
78	Multibus signal INT5/
79	Multibus signal INT4/
8Ø	Multibus signal INT3/
81	Multibus signal INT2/
82	Multibus signal INT1/
83	Multibus signal INTØ/
85	Pullup resistor R13 for unused inputs of U27
86	pin 3,4 P2
87	pin 6 P2
88	pin 7,8 P2
89	pin 11,12 P2
9Ø	pin 13 P2
91	pin 15,16 P2
92	pin 17 P2
93	pin 18 P2
94	pin 19 P2
95	pin 2Ø P2
96	pin 23,24 P2
97	pin 25,26 P2
98	pin 27 P2
99	pin 28 P2
1ØØ	pin 29 P2
1Ø1	pin 3Ø P2
1Ø2	pin 32 P2
1Ø3	pin 38 P2
1Ø4	pin 42 P2
1Ø5	pin 44 P2
1Ø6	pin 46 P2
1Ø7	pin 49 P2
1Ø8	pin 54 P2
1Ø9	pin 55 P2

110	pin 33 P2
111	pin 34 P2
112	pin 36 P2
113	pin 40 P2
114	pin 41 P2
115	pin 45 P2
116	pin 47 P2
117	pin 52 P2
118	pin 53 P2
119	pin 58 P2
120	pin 60 P2
121	pin 5 P2
122	pin 10 P2
123	pin 9 P2
124	pin 14 P2
125	pin 31 P2
126	pin 35 P2
127	pin 37 P2
128	pin 39 P2
129	pin 43 P2
130	pin 48 P2
131	pin 50 P2
132	pin 51 P2
133	pin 56 P2
134	pin 57 P2
135	pin 59 P2

Table 5.1
Jumper Pin Allocation

Could we have your comments, please.

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